ABSTRACT OF THE DISCLOSURE

A pipelined adaptive decision feedback equalizer (DFE). The pipelined ADFE comprises a pre-processing unit, an adder, a feedback filter (FBF), a slicer, a delay unit, a weight-update block and a mapping circuit. The pre-processing unit comprising a plurality of PP coefficients filters a signal received from a channel, and outputs a PP output signal to the adder. The slicer outputs a decision signal based on an added signal output from the adder. The FBF comprising a plurality of FBF coefficients receives the decision signal and generates a FBF output signal to the delay unit. The delay unit outputs a delayed signal to the adder. The weight-update block adapts the FBF coefficients to cancel the post-cursor ISI and selects a plurality of coefficients from the FBF coefficients. The mapping circuit translates the FFF coefficients by a predetermined method to generate the PP coefficients output to the pre-processing unit.